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Claims

[c1] A deep trench capacitor in a monocrystalline semiconductor substrate, said capacitor comprising: (i) a buried plate in said substrate about an exterior portion of a trench in said substrate, (ii) a node dielectric about at least a lower interior portion of said trench, (iii) a trench electrode in said trench, and (iv) a conductive strap extending away from said trench electrode, the conductive strap being electrically connected to the trench electrode and the monocrystalline substrate, said capacitor further comprising (v) a Si-C barrier layer between said monocrystalline substrate and said trench electrode.

[c2] The capacitor of claim 1, further comprising an oxide collar about an upper interior region of said trench and disposed below said conductive strap.

[c3] The capacitor of claim 1, wherein said Si-C barrier layer is located at an interface between said trench electrode and said conductive strap.

[c4] The capacitor of claim 1, wherein said Si-C barrier layer is located at an interface between said conductive strap and said monocrystalline substrate.

[c5] The capacitor of claim 4, wherein the interface is located below a vertical transistor.

[c6] The capacitor of claim 1, wherein said Si-C barrier layer has a thickness of about 10nm.

[c7] The capacitor of claim 1, wherein said conductive strap is a buried strap.

[c8] The capacitor of claim 1, wherein said conductive strap comprises amorphous silicon.

[c9] The capacitor of claim 1, wherein said trench electrode comprises doped polycrystalline silicon.

[c10] The capacitor of claim 3, further comprising an additional Si-C barrier layer located at an interface between said conductive strap and said monocrystalline substrate.

[c11] A method of forming a deep trench capacitor in a monocrystalline semiconductor substrate, said method comprising:
(a) providing a monocrystalline semiconductor substrate having (i) a buried plate about an exterior portion of trench in said substrate, (ii) a node dielectric about at least a lower interior portion of said trench, and (iii) a trench electrode in said trench;

(b) removing an upper portion of said trench electrode to provide space for a conductive strap, thereby exposing a trench electrode surface and a vertical substrate surface;
(c) reacting, in the presence of an electric field, said exposed surface of the electrode and the substrate about said space with a compound containing carbon to form a Si-C barrier layer on at least said substrate surface; and
(d) filling said space over said electrode layer with a conductive strap material.

[c12] A method according to claim 11, wherein said step of removing an upper portion is performed with a reactive ion etch on oxide and said compound containing carbon is the etchant gas.

[c13] A method according to claim 12, wherein a power level of RF power is above a threshold value.

[c14] A method according to claim 13, wherein said power level is maintained at the end of an oxide removal etching process.

[c15] The method of claim 11, further comprising removing said Si-C layer from said trench electrode surface before step (d).

[c16] The method of claim 11, wherein step (c) is performed at about 20 to 80 degrees Centigrade.

[c17] The method of claim 11 wherein step (a) further comprises providing an oxide collar about an upper interior region of said trench, and step (b) further comprises removing a portion of said oxide collar and thereby exposes a vertical surface of said substrate.

[c18] A method according to claim 18, wherein said step of removing an upper portion is performed with a reactive ion etch on oxide and said compound containing carbon is the etchant gas.

[c19] A method according to claim 18, wherein a power level of RF power is above a threshold value.